

Z10PE-D16 series Repair Guide

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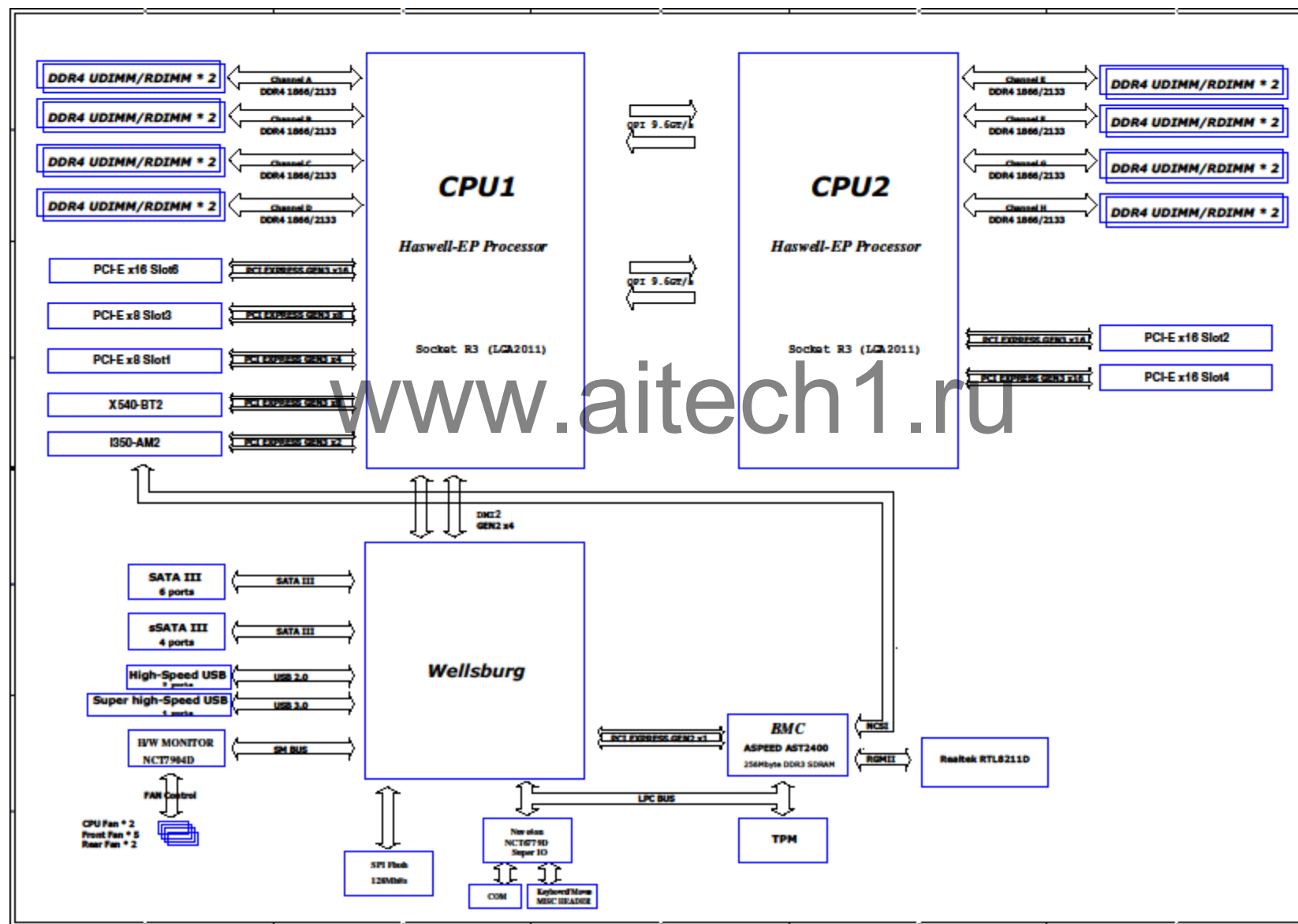
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2014/10/6



Package

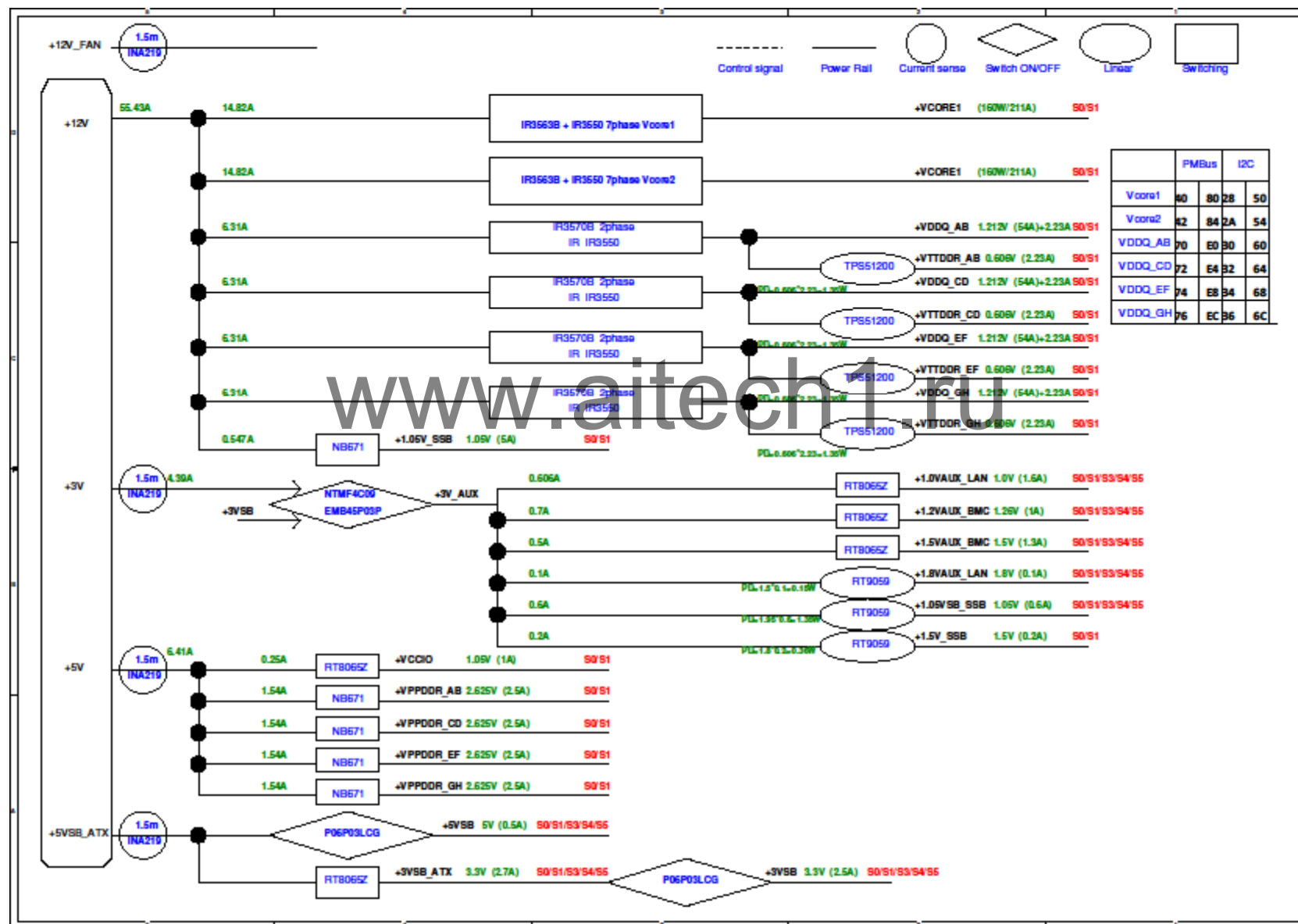
Block Diagram





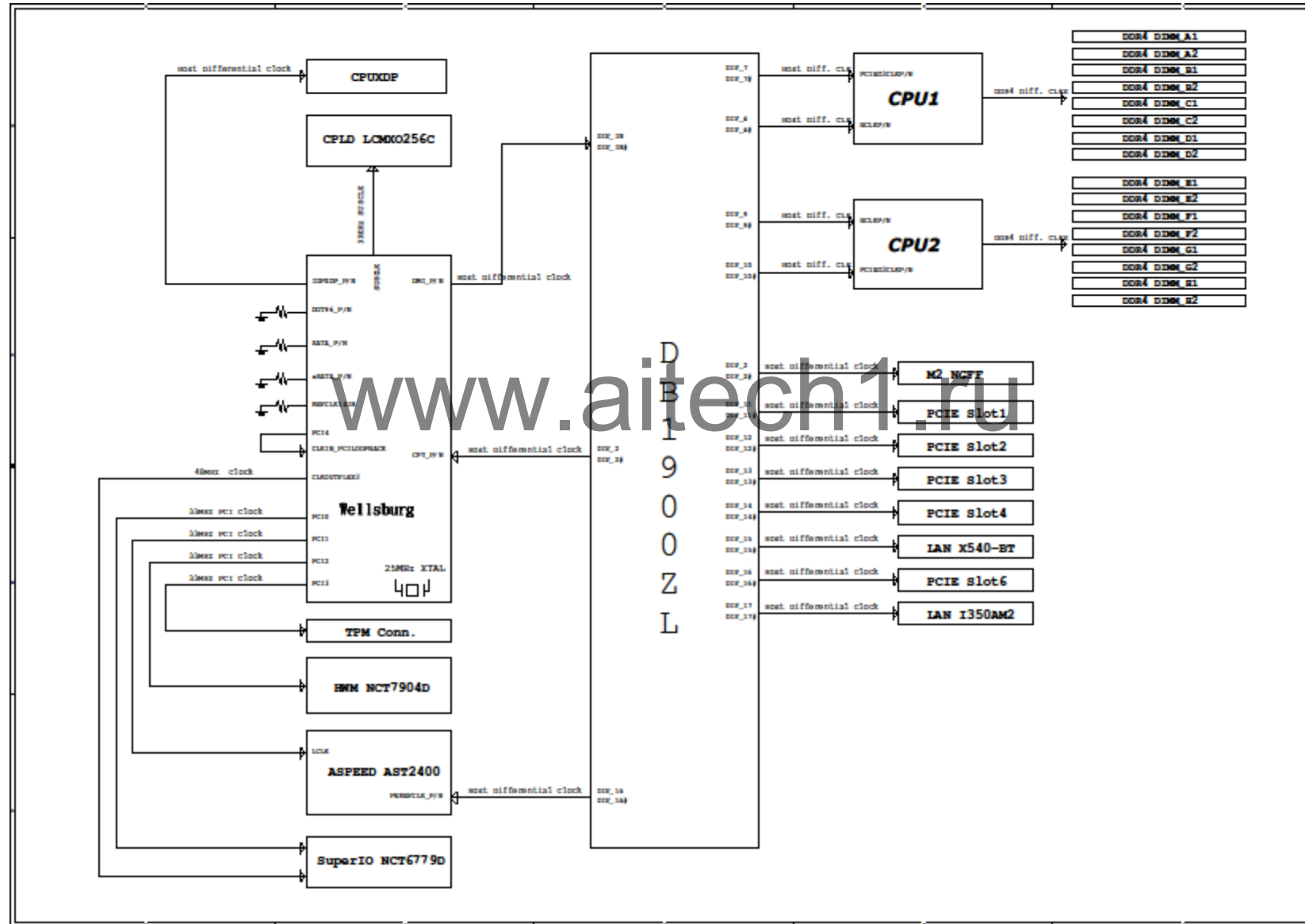
Package

Power Flow





Clock Distribution





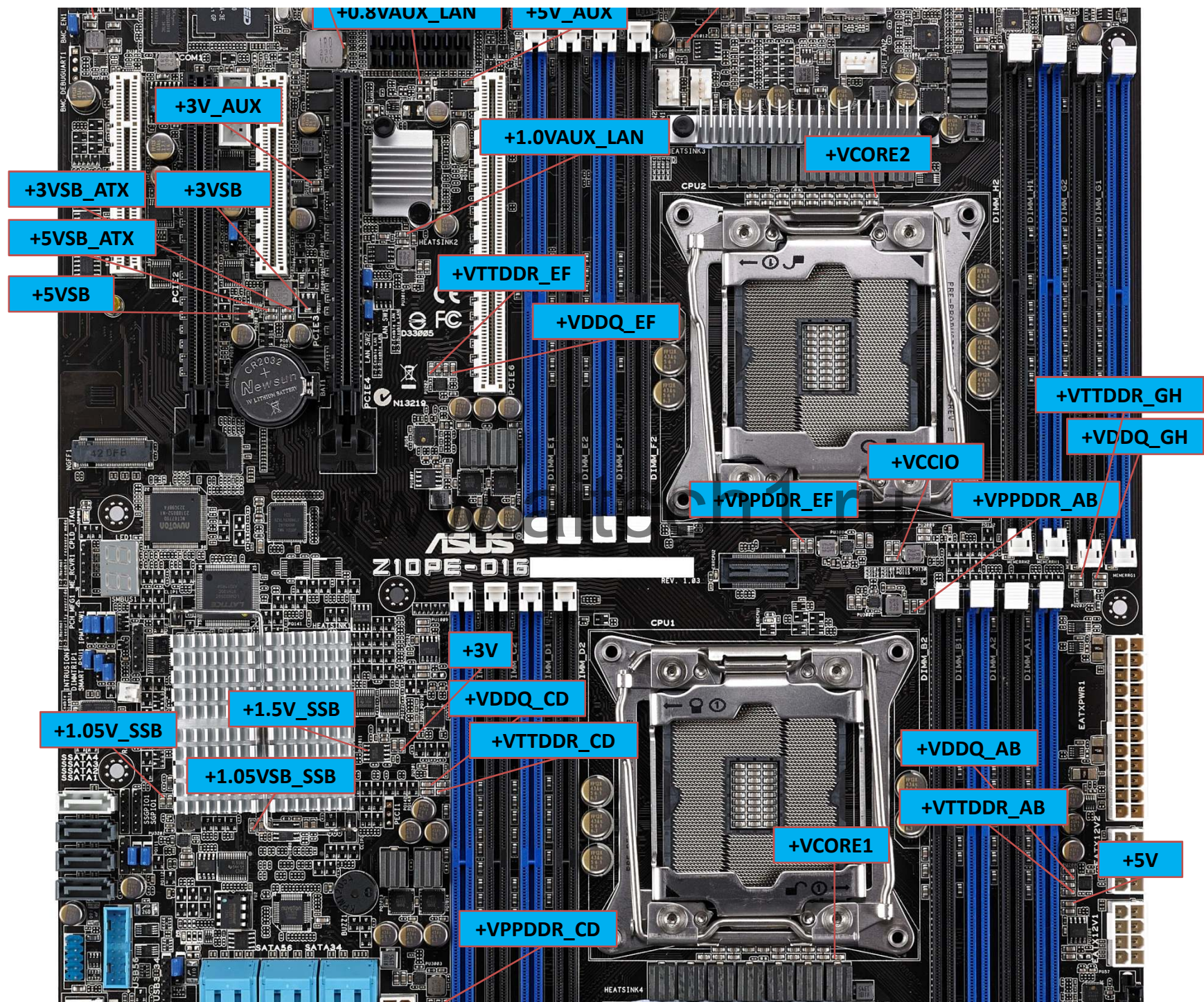
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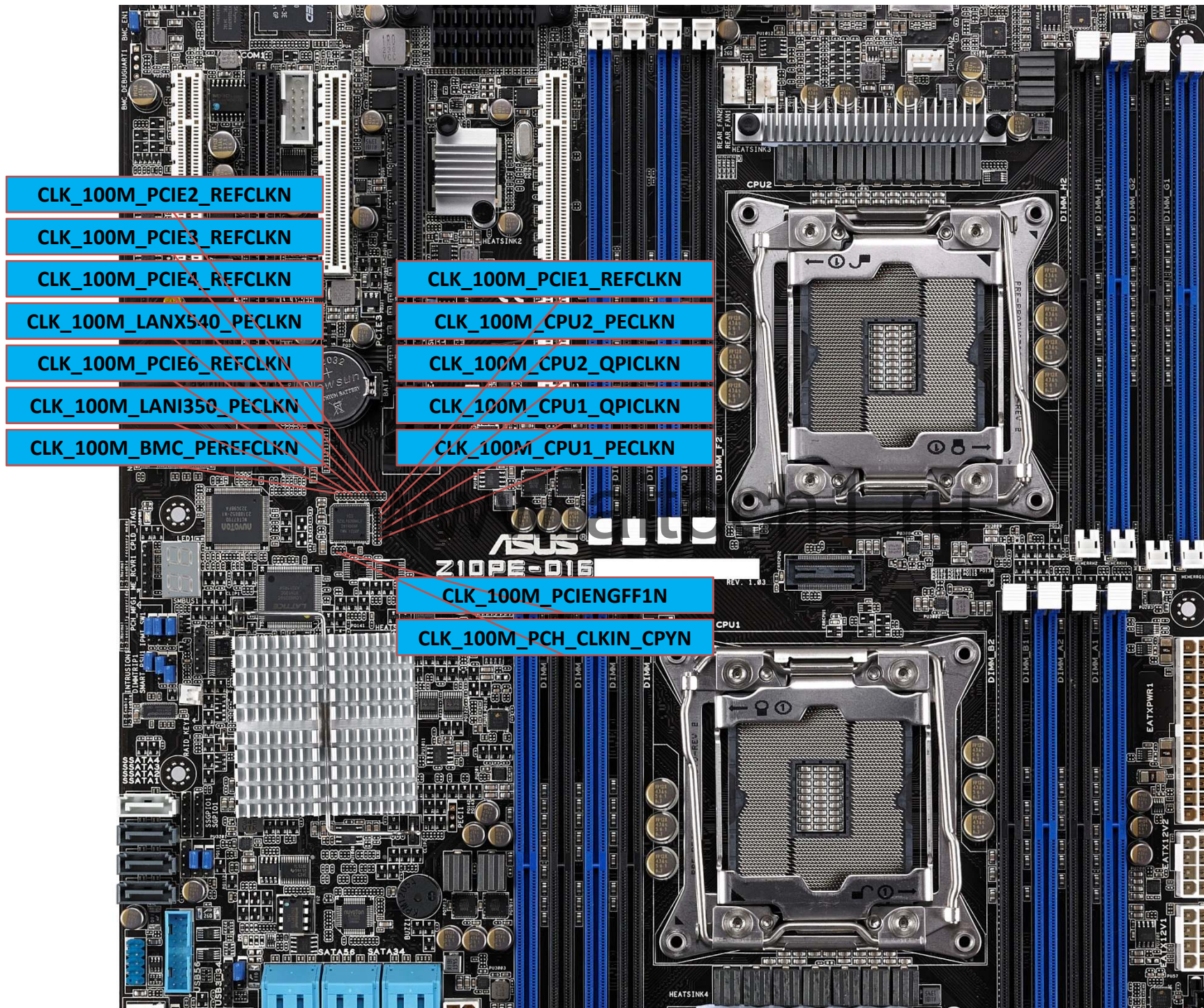
Power Sequence

Power Sequence

```
1. VDDT
1 → 2 t = 0 sec
2. PCH_RSTOUT#
2. CPU0_A000CE/CPU0_RESET#
3. Power Flag
4. +VDD0_A0T0
5 → 6 t = 0 sec
6. +VDD0_A0T0
6 → 7 t = 10 sec
7. +VDD0_A0T0_PWDN
7 → 8 t = 85 sec
8. PCH_RSTIN#
8 → 9 t = 0.7 sec
9. +VDD0
9 → 10 t = 0 sec
10. +VDD0
11. +VDD_A0T0(VDD)
11 → 12 t = 100 sec
12. +VDD0T0_SMC
+VDD0T0_SMC (SMD)
12 → 13 t = 100 sec
13. +VDD0T0_SMC
+VDD0T0_SMC (SMD)
13 → 14 t = 10.5 sec
14. +VDD0T0_SMC_PWDN
15. SMC_RSTIN#
SMC_RSTIN#
15 → 16 t = 100 sec
16. SMC_RSTIN#
16 → 17 t = 100 sec
17. PCH_RSTIN#
18. +VDD0T0_SMC
+VDD0T0_SMC_PWDN
19. CPU0_A000CE
CPU0_P000
20. PCH_RSTIN#
21. PCH_RSTIN#
22. N_VDD_PWDN#
22 → 23 t = 64 sec
23. SMC_RSTIN#
24. N_PCH_RSTIN# (SMP_RST)
24 → 25 t = 10 sec
25. PCH_RSTIN#
25 → 26 t = 10 sec
26. PCH_RSTIN#
27. SMC_RSTIN#
28. AT0P000
SMC_AT0P000
29. +VDD/VDDT/VDDT/-LDP
29 → 30 t = 100 → 500 sec
30. AT0P000
31. SMC_RSTIN#
32. +VDD_A0T0(SMD)
33. +VDD_SMC
34. +VDD_SMC_PWDN
35. CPU0_VDD0T0_SMC
36. +VDD0T0
37. +VDD0T0_PWDN
38. +VDD_SMC
39. +VDD_SMC_PWDN
40. +VDD0T0_A0T0/VDDT/VDDT
41. CPU0_SMC_CPU0_SMC
CPU0_SMC_CPU0_SMC
+VDD0T0_A0T0/VDDT/VDDT_PWDN
42. +VDD0T0_A0T0/VDDT/VDDT
43. CPU0_VDD0T0_SMC
CPU0_VDD0T0_SMC
44. +VDD0T0/VDD0T0
45. +VDD0T0_PWDN
+VDD0T0_PWDN
```

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CLK_100M_PCIE2_REFCLKN

CLK_100M_PCIE3_REFCLKN

CLK_100M_PCIE4_REFCLKN

CLK_100M_LANX540_PECCLKN

CLK_100M_PCIE6_REFCLKN

CLK_100M_LAN1350_PECCLKN

CLK_100M_BMC_PERECLKN

CLK_100M_PCIE1_REFCLKN

CLK_100M_CPU2_PECCLKN

CLK_100M_CPU2_QPICKLN

CLK_100M_CPU1_QPICKLN

CLK_100M_CPU1_PECCLKN

CLK_100M_PCIENGFF1N

CLK_100M_PCH_CLKIN_CPYN

