Z10PE-D16 series
Repair Guide

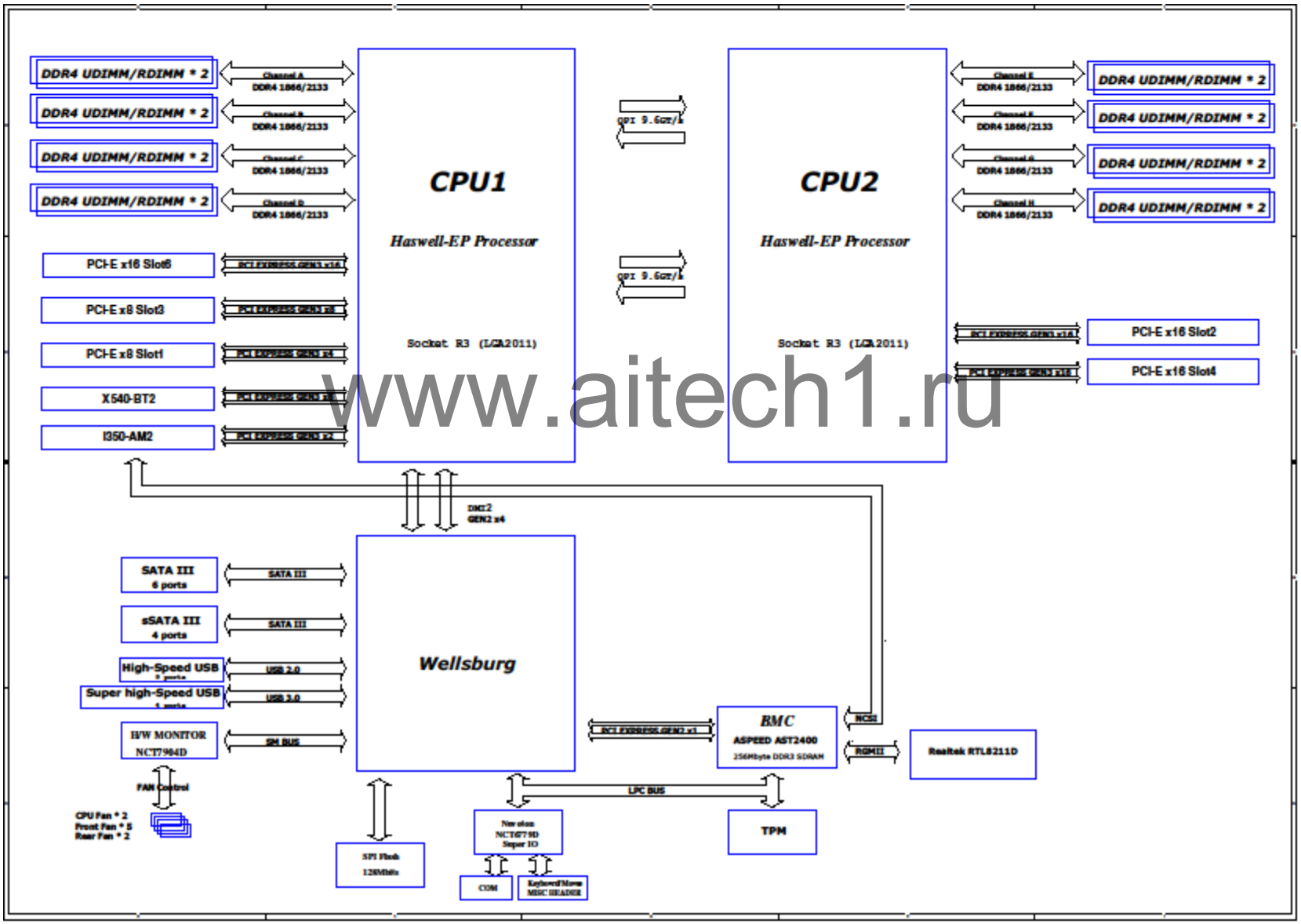
Editor-P.P Pam(潘竑蒼)

Manager-Ryan Hung(洪志安)

2014/10/6

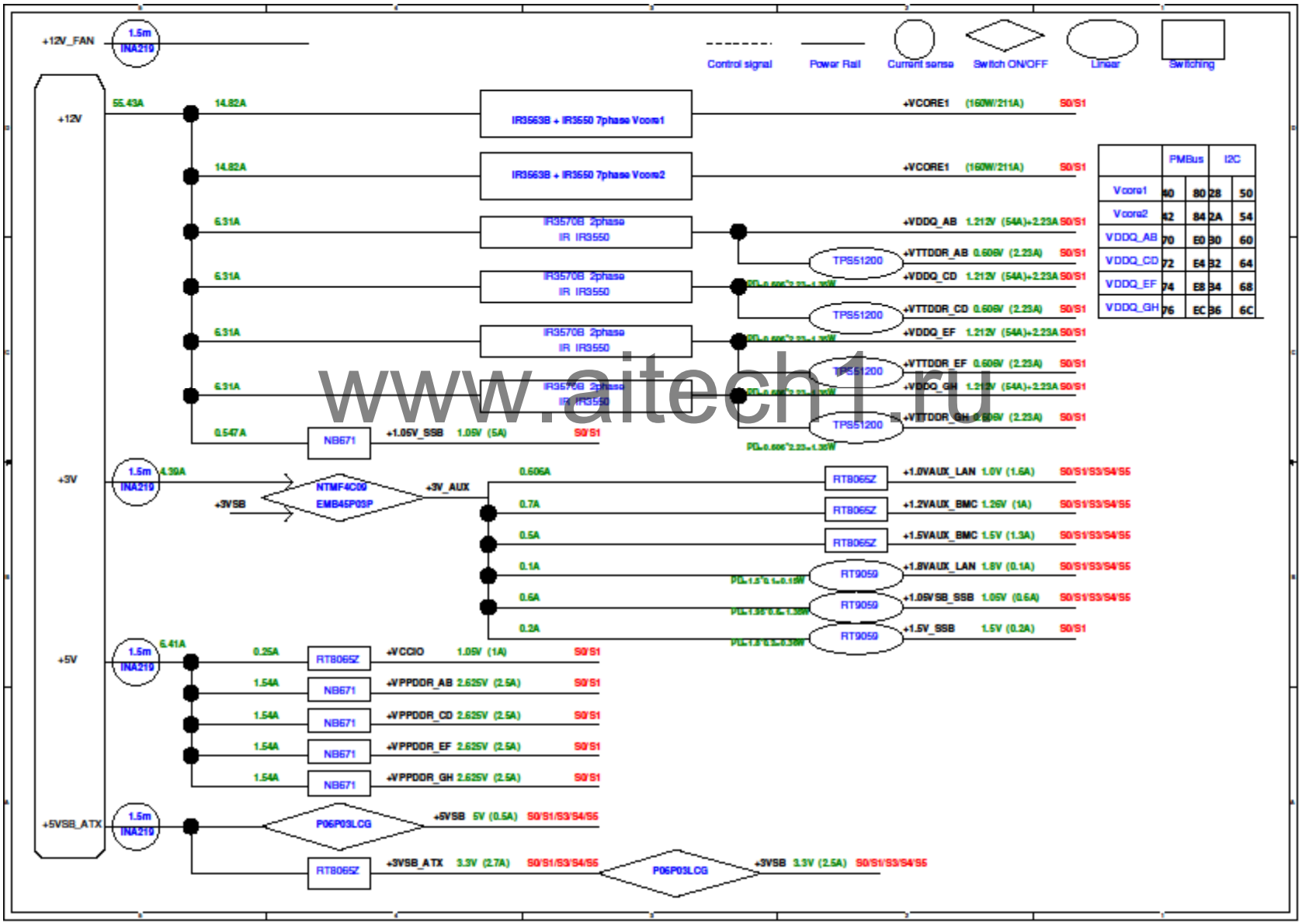
Package

Block Diagram



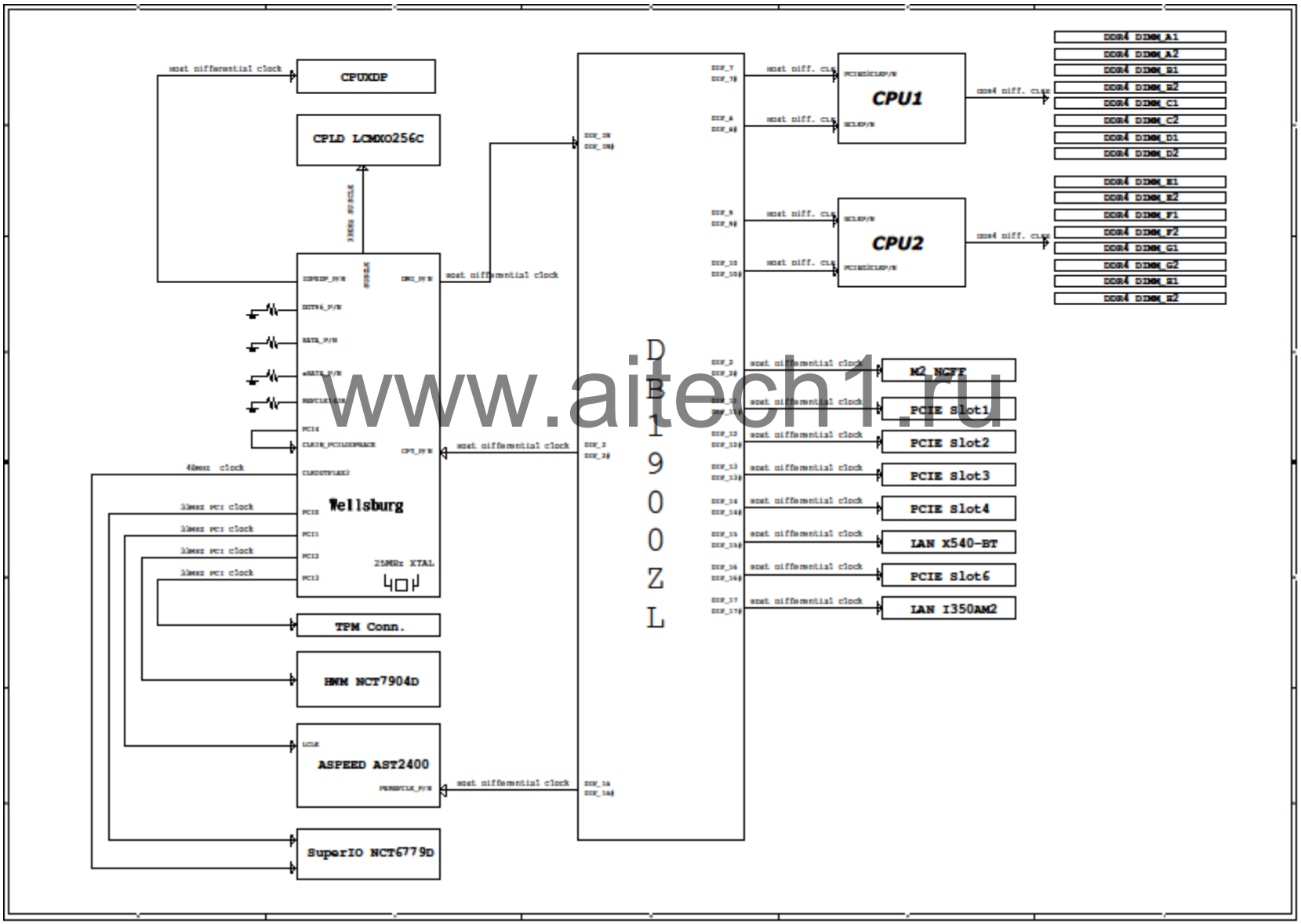
Package

Power Flow



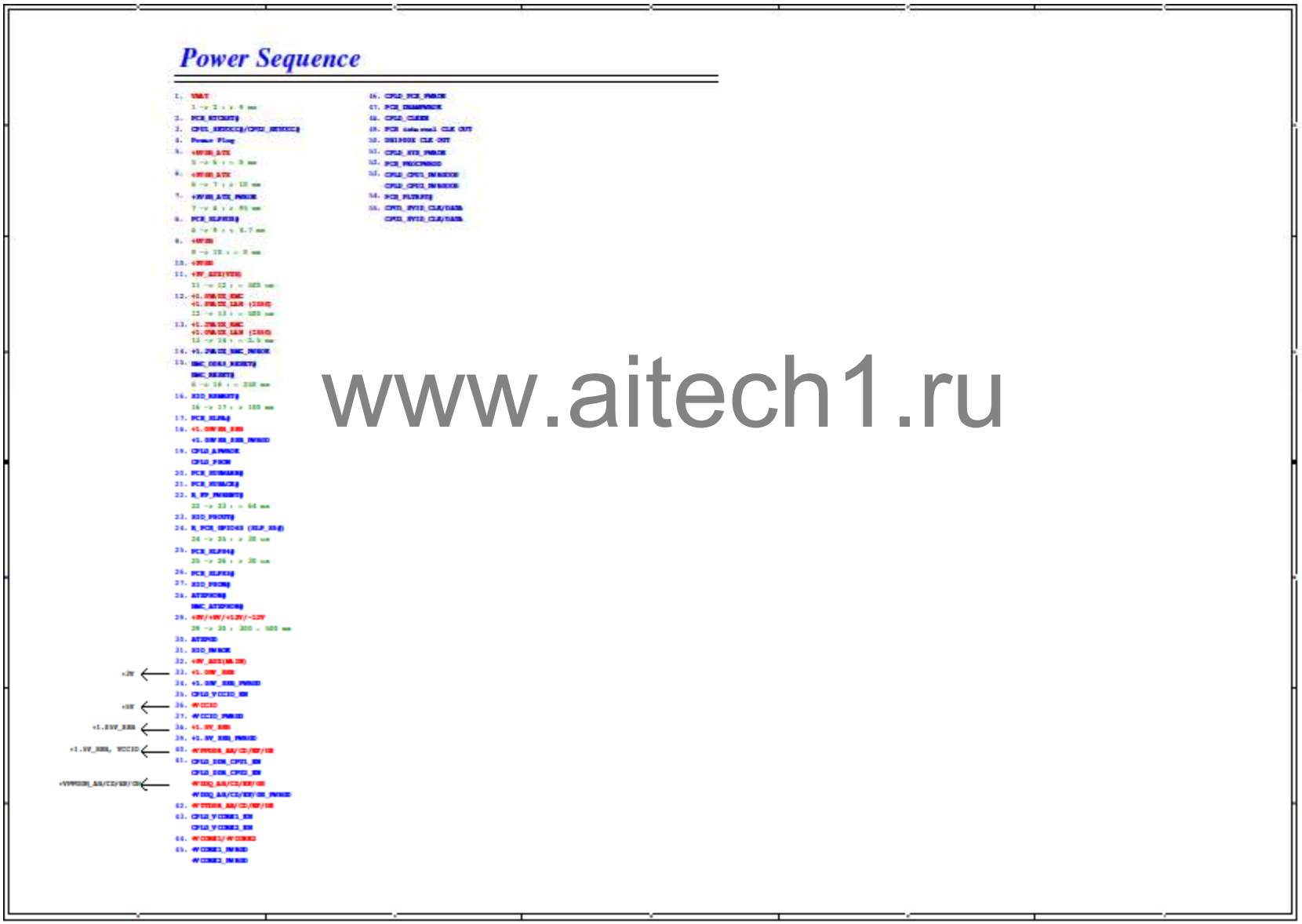
Package

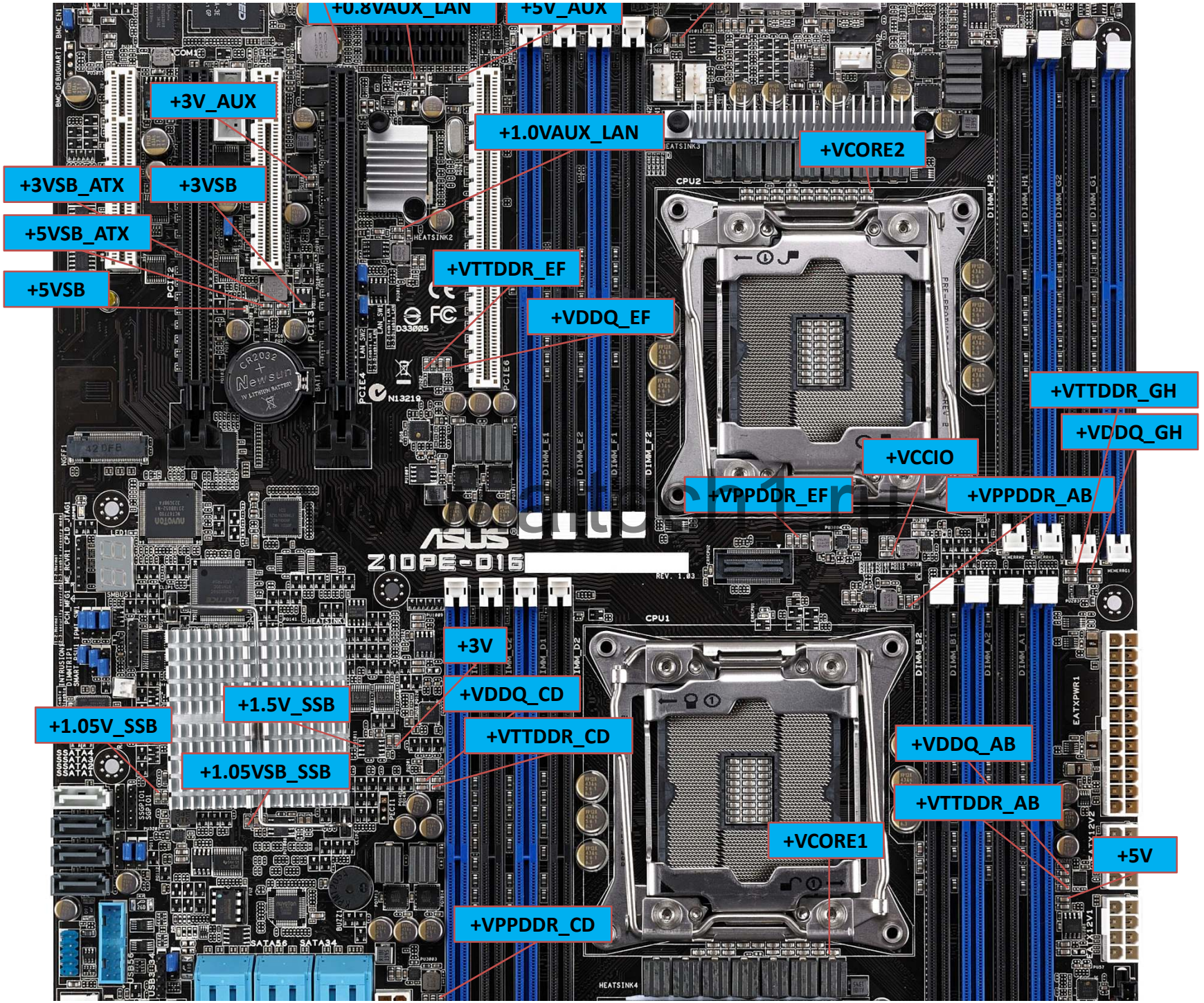
Clock Distribution

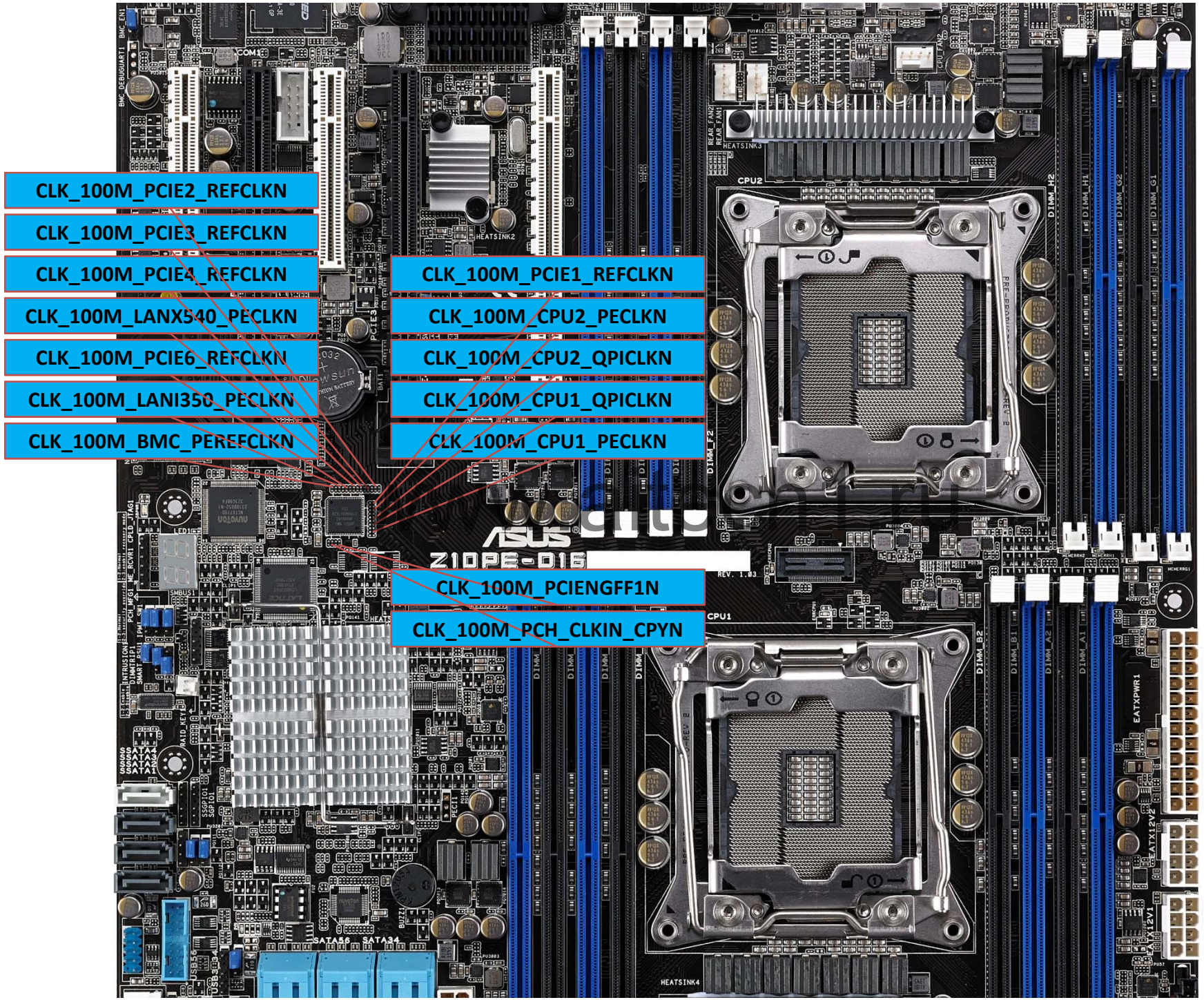


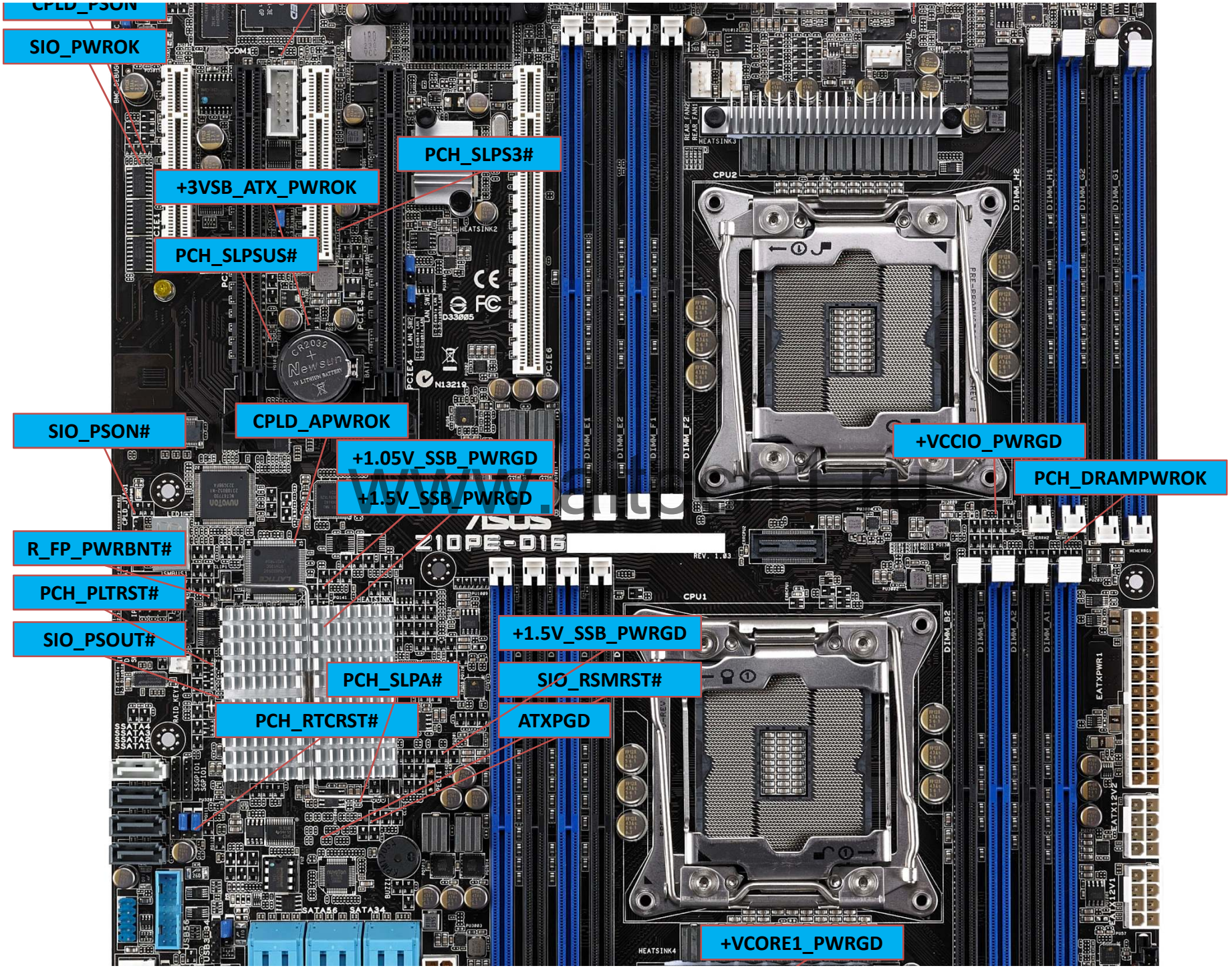
Package

Power Sequence




+0.8VAUX_LAN
+5V_AUX
+3V_AUX
+1.0VAUX_LAN
+VCORE2
+3VSB_ATX
+3VSB
+5VSB_ATX
+5VSB
+VTTDDR_EF
+VDDQ_EF
+VTTDDR_GH
+VDDQ_GH
+VCCIO
+VPPDDR_EF
+VPPDDR_AB
+3V
+VDDQ_CD
+1.5V_SSB
+1.05V_SSB
+VTTDDR_CD
+VDDQ_AB
+1.05VSB_SSB
+VTTDDR_AB
+VCORE1
+5V
+VPPDDR_CD
ASUS
Z10PE-D16
CPU1
CPU2


CLK_100M_PCIE2_REFCLKN
CLK_100M_PCIE3_REFCLKN
CLK_100M_PCIE4_REFCLKN
CLK_100M_LANX540_PECLKN
CLK_100M_PCIE6_REFCLKN
CLK_100M_LANI350_PECLKN
CLK_100M_BMC_PEREFCLKN
CLK_100M_PCIE1_REFCLKN
CLK_100M_CPU2_PECLKN
CLK_100M_CPU2_QPICLKN
CLK_100M_CPU1_QPICLKN
CLK_100M_CPU1_PECLKN
CLK_100M_PCIENGFF1N
CLK_100M_PCH_CLKIN_CPYN
ASUS
Z10PE-D16
CPU1
CPU2
HEATSINK2
HEATSINK3
HEATSINK4


CPLD_PSON
SIO_PWROK
PCH_SLPS3#
+3VSB_ATX_PWROK
PCH_SLPSUS#
SIO_PSON#
CPLD_APWROK
+1.05V_SSB_PWRGD
+1.5V_SSB_PWRGD
+VCCIO_PWRGD
PCH_DRAMPWROK
R_FP_PWRBNT#
PCH_PLTRST#
SIO_PSOUT#
PCH_SLPA#
PCH_RTCRST#
+1.5V_SSB_PWRGD
SIO_RSMRST#
ATXPGD
+VCORE1_PWRGD
Z10PE-D16
CPU1
CPU2